

Claims:

1        An integrated circuit comprising: a gate array architecture;  
2        said gate array architecture including a semiconductor substrate having a plurality of N-type  
3        diffusion regions and P-type diffusion regions; said diffusion regions having partially overlying  
4        polysilicon landing sites to form N-type and P-type transistors;  
5                wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and  
6        P-type transistors and larger N- and P-type transistors.

1        2.        The integrated circuit of claim 1, wherein the ratio between the two distinct transistor sizes  
2        is on the order of one-third.

1        3.        The integrated circuit of claim 2, wherein the ratio between the capacitance of the larger  
2        and smaller relatively sized transistors is on the order of one-third.

1        4.        The integrated circuit of claim 1, wherein said partially overlying polysilicon landings for the  
2        smaller and larger transistors are not connected.

1        5.        The integrated circuit of claim 4, and further comprising an interconnect overlying said gate  
2        array architecture;  
3                the interconnect being adapted to connect the transistors of the gate array architecture to  
4        form a flip-flop.

1        6.        The integrated circuit of claim 5, wherein the interconnect is further adapted to connect  
2        the transistors of the gate array architecture so that the internal clock buffers of the flip-flop are  
3        formed from the smaller transistors.

1        7.        The integrated circuit of claim 6, wherein said gate array architecture is repeated in said  
2        integrated circuit.

1        8.        The integrated circuit of claim 6, wherein said integrated circuit is incorporated in a  
2        communications device.

1        9.        The integrated circuit of claim 6, wherein said integrated circuit is attached to a  
2        motherboard.

1        10.       The integrated circuit of claim 9, wherein said integrated circuit is incorporated in a  
2        personal computer.

1        11.       The integrated circuit of claim 10, wherein said personal computer comprises one of a  
2        laptop and a desktop computer.

1        12.       The integrated circuit of claim 1, wherein successive rows of small diffusion regions are  
2        followed by successive rows of regular-sized diffusion regions;  
3                wherein immediately successive rows within similarly-sized diffusion regions have opposite  
4        polarity.

1 13. A method of fabricating an integrated circuit chip comprising:  
2 processing a semiconductor substrate to form a gate array architecture of transistors in the  
3 substrate, the gate array architecture comprising a plurality of N-type diffusion regions and P-type  
4 diffusion regions; said diffusion regions having partially overlying polysilicon landing sites to form  
5 N-type and P-type transistors;  
6 wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and  
7 P-type transistors and larger N- and P-type transistors.

1 14. The method of claim 13, wherein said semiconductor substrate comprises a silicon  
2 substrate.

1 15. The method of claim 14, wherein processing said silicon substrate to form a gate array  
2 architecture comprises:  
3 forming said partially overlying polysilicon landings so that said landings for the smaller and  
4 larger transistors are not connected.

1 16. The method of claim 15, wherein the ratio between the two distinct transistor sizes is on  
2 the order of one-third.

1 17. The method of claim 16, wherein the ratio between the capacitance of the larger and  
2 smaller relatively sized transistors is on the order of one-third.

1 18. The method of claim 15, and further comprising:  
2 forming a metallization interconnect overlying said gate array architecture.

1 19. The method of claim 18, wherein forming a metallization interconnect comprises forming a  
2 metallization interconnect that connects the transistors of the gate array architecture to form a  
3 flip-flop.

1 20. The method of claim 19, wherein forming a metallization interconnect comprises forming  
2 an interconnect that connects the transistors of the gate array architecture so that the internal  
3 clock buffers of the flip-flop are formed from the smaller transistors.

1 21. An article comprising: a storage medium, said storage medium having instructions stored  
2 thereon, said instructions, when executed, resulting in the capability to design the layout of an  
3 integrated circuit chip for fabrication, the integrated circuit chip including a gate array architecture,  
4 the gate array architecture comprising a plurality of N-type diffusion regions and P-type diffusion  
5 regions; said diffusion regions having partially overlying polysilicon landing sites to form N-type  
6 and P-type transistors;  
7 wherein the regions are relatively-sized to form two distinct transistor sizes, smaller N- and  
8 P-type transistors and larger N- and P-type transistors.

1 22. The article of claim 21, wherein said instructions, when executed, result in the capability to  
2 design the layout of the gate array architecture, wherein the ratio between the two distinct  
3 transistor sizes is on the order of one-third.

1 23. The article of claim 22, wherein said instructions, when executed, result in the capability to  
2 design the layout of the gate array architecture, wherein said partially overlying polysilicon  
3 landings for the smaller and larger transistors are not connected.

1 24. The article of claim 23, wherein said instructions, when executed, result in the capability to  
2 design the layout of a metallization interconnect overlying said gate array architecture.

1 25. The article of claim 24, wherein said instructions, when executed, result in the capability to  
2 design the layout of a metallization interconnect overlying said gate array architecture, wherein  
3 said metallization interconnect couples the transistors of the gate array architecture to form a flip-  
4 flop.

26. The article of claim 25, wherein said instructions, when executed, result in the capability to  
design the layout of a metallization interconnect overlying said gate array architecture that  
connects the transistors of the gate array architecture so that the internal clock buffers of the flip-  
flop are formed from the smaller transistors.

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